

In re Patent Application of:
GARNIER ET AL.
Serial No. 09/499,060
Filing Date: February 4, 2000

E1
End

charging current to be proportional to a square of a ratio of the second resistance and the first resistance, said first and second resistances having a same type technology.

15. (Three Times Amended) An integrated circuit voltage ramp generator produced using semiconductor technology and comprising:

a capacitance; and

a charging circuit connected to said capacitance and

E2

comprising

a current generator having a first resistance, and

a degenerate current mirror circuit connected to said current generator and to said capacitance, said degenerate current mirror circuit having a second resistance for generating a capacitance charging current that is proportional to a square of a ratio of the second resistance and the first resistance, said first and second resistances having a same type technology.

21. (Three Times Amended) An integrated circuit current ramp generator produced using semiconductor technology and comprising:

E3
Cont.

a voltage ramp generator comprising

a capacitance, and

a charging circuit connected to said capacitance and comprising

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a current generator having a first resistance, and

23
F2
END
a circuit connected to said current generator and to said capacitance, said circuit having a second resistance and enabling a capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance, said first and second resistances having a same type technology; and

a conversion circuit connected to said voltage ramp generator for generating a current ramp.

24
F4
24. (Twice Amended) An integrated circuit current ramp generator according to Claim 21, wherein said charging circuit comprises a degenerate current mirror circuit.

29. (Three Times Amended) An integrated circuit current ramp generator produced using semiconductor technology and comprising:

a voltage ramp generator comprising

a capacitance having a first resistance, and

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F5
Cont.
a charging circuit connected to said capacitance and comprising

a current generator, and

a degenerate current mirror circuit connected to said current generator and to said capacitance, said degenerate current mirror circuit having a second resistance for generating a capacitance charging current that